Customer No.: 31561
Docket No.: 13137-US-PA
Application No.: 10/710,844

REMARKS

Claim Rejections – 35 U.S.C. § 103

The Office Action rejected claims 1-4 under 35 U.S.C. 103(a) as being unpatentable over Zhang (U.S. Patent No. 6,855,954) in view of Cho et al. (U.S. Patent No. 6,391,693).

In response to the rejection to claims 1-4 under 35 U.S.C. 103(a) as being unpatentable over Zhang (U.S. Patent No. 6,855,954) in view of Cho et al. (U.S. Patent No. 6,391,693), Applicant hereby otherwise traverses this rejection. As such, Applicant submits that claims 1-4 are now in condition for allowance.

With respect to claim 1, as originally filed, recites in parts:

A low-temperature polysilicon thin film transistor ..., comprising:

... a patterned silicon layer disposed on the gate dielectric layer and over the gate, wherein the patterned silicon layer comprises a polysilicon channel region and ***an amorphous silicon hot carrier restrain region*** adjacent thereto ... (Emphasis added)

Applicant submits that neither Zhang (U.S. Patent No. 6,855,954), nor Cho et al. (U.S. Patent No. 6,391,693) teaches, discloses or suggests "a patterned silicon layer comprising a polysilicon channel region and ***an amorphous silicon hot carrier restrain***

region adjacent thereto ... (Emphasis added)" required by the present invention as set forth in claim 1. Applicant notes that the Examiner admits that "Zhang (U.S. Patent No. 6,855,954) fails to disclose the required configuration where the central portion of the channel semiconductor layer is polysilicon and the side portions are amorphous" (Paragraph 2, Page 2 of the instant Office Action). Then the Examiner cites Cho et al. (U.S. Patent No. 6,391,693) as a second reference to modify Zhang (U.S. Patent No. 6,855,954) to render the present invention as set forth in claim 1 an obvious case. However, Cho et al. (U.S. Patent No. 6,391,693) fail to teach or suggest that "the patterned silicon layer of the claimed invention comprises a polysilicon channel region and ***an amorphous silicon hot carrier restrain region*** adjacent thereto".

In re paragraph [0038] of the present invention, Applicants disclosed that "... Because the first patterned amorphous silicon layer 206a under the patterned insulating layer 208 is undoped, the first patterned amorphous silicon layer 206a under the overlap of the second patterned amorphous silicon layer 210 and the patterned insulating layer 208 becomes an ***undoped amorphous silicon hot carrier restrain region 216***. The fabrication method of the present invention precisely defines the position of the polysilicon region and the amorphous silicon region. Due to the high impedance of the amorphous silicon, the ***amorphous silicon hot carrier restrain region 216*** effectively reduces leakage currents of the transistor. In other words, the leakage current is reduced. On the contrary, in re U.S. Patent No. 6,391,693, Cho et al. disclosed that "And then, as shown in FIG. 2C, source and

drain impurities 17 are ion-implanted in the amorphous channel layer 14a of both sides of the ion stopper 15. Herein, the impurities 17 are not implanted to the channel layer 14a formed in the lower portion of the ion stopper 15. The impurities 17 are implanted at a dose of 10.sup.11.about.10.sup.19 ions/cm.sup.3 regardless of the types of impurities, i.e. N type or P type. As shown in FIG. 2D, ***the amorphous channel layer 14a is annealed by exposing a laser beam so that the implanted impurities 17 in the amorphous channel layer 14a are activated and the amorphous channel layer 14a becomes polysilicon***. Herein, the laser beam can be emitted from the front side, from back side or from both front and back sides. ***According to the laser annealing process, the amorphous channel layer 14a becomes poly-channel layer 14 and the impurities 17 are activated thereby forming junction regions 18a, 18b, 18c***. Herein, the substantial source and drain regions are the junction regions 18a, 18b in the outer positions. Further, the junction regions 18c between the gate electrodes 12 become an auxiliary junction region". As described above, Applicant submits that the junction regions 18a, 18b and 18c disclosed by Cho et al. are polysilicon with source and drain impurities 17. In other words, the junction regions 18a, 18b and 18c disclosed by Cho et al. are not amorphous silicon portions and cannot function as a ***hot carrier restrain region***. Obviously, Cho et al. fail to teach or suggest ***the amorphous silicon hot carrier restrain region*** recited in claim 1.

Therefore, while neither Zhang (U.S. Patent No. 6,855,954), nor Cho et al. (U.S. Patent No. 6,391,693) teaches, discloses or suggests such a required "***amorphous silicon***

hot carrier restrain region" as set forth in claim 1, claim 1 is submitted to be novel and unobvious over Zhang (U.S. Patent No. 6,855,954) and Cho et al. (U.S. Patent No. 6,391,693), and should be allowable. *(MPEP §2143.03)*

Claims 2-4 depend from claim 1, and if claim 1 is allowable, claim 2-4 should be also allowable.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-4 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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